ACS Photonics

pubs.acs.org/journal/apchd5

Article

Low-Loss Nanophotonic Devices with Chip-Level Uniformity and Integrated Color Centers in an SiC-On-Insulator

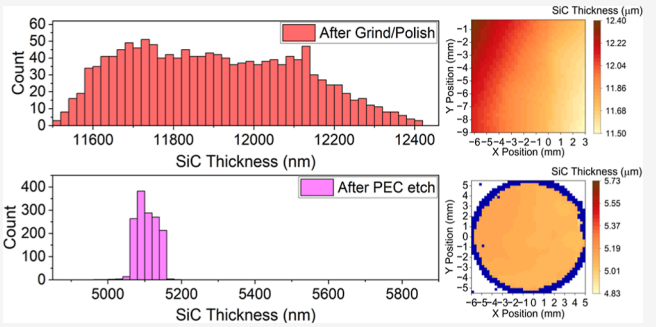
Jason Lipton,* Brett Yurash, Adam Sorensen, John Vajo, Samuel Whiteley, Tong Wang, Biqin Huang, Xiwei Bai, Adrian Portales, Sam Rubin, Judas Strayer, Jason Graetz, and Shanying Cui*

Cite This: https://doi.org/10.1021/acsphotonics.4c01834

Read Online

ACCESS | Metrics & More | Article Recommendations | Supporting Information

ABSTRACT: 4H−SiC is a promising material platform for quantum photonic integrated circuits due to its wide bandgap, high refractive index, and variety of optically addressable defects, while being compatible with CMOS fabrication processes. However, it is currently not possible to fabricate chip-scale photonic integrated circuits with integrated color centers due to nonuniformity of SiC thickness arising from the SiC-on-insulator fabrication process. We apply the concept of dopant-selective photoelectrochemical etching to a SiC-on-insulator stack for a highly effective total thickness variation (TTV) reduction. We show a reduction of SiC TTV by a factor of 7 through selectively etching a high-TTV sacrificial n-type layer, to stop on an epitaxially defined intrinsic layer. Fabricated photonic devices on selectively etched SiCOI exhibit a high yield of optical elements while maintaining a record low propagation loss for 920 nm single-mode optical elements in SiC (2 dB/cm). Finally, we show etch process compatibility with color centers through the measurement of zero phonon line emission from ensemble divacancy defects into our fabricated waveguides. This work represents the first successful demonstration of a TTV reduction method in SiCOI that is compatible with color center emission, marking a significant advancement toward scalable 4H−SiC-on-insulator integrated photonics for quantum technologies.



KEYWORDS: *silicon carbide, quantum photonic devices, spin defects, photoelectrochemical etching*

INTRODUCTION

The 4H−SiC-on-insulator (SiCOI) has gained attention as a candidate integrated photonic platform for quantum technologies, with several seminal demonstrations to that end in recent years.[1−3] 4H−SiC is attractive for chip-integrated quantum networking components for a few reasons; it hosts color centers such as the divacancy with long spin coherence times that interface with photons near telecommunication wavelengths,[1,4−6] it exhibits strong χ^2 nonlinearity,[7] and it has a large wafer-scale supply chain, which is amenable to CMOS foundry processes. However, challenges in uniform thin film fabrication make translation of 4H−SiC's intrinsic properties to SiC-on-insulator (SiCOI) devices impractical at wafer scale with current methods.

In the most common SiCOI fabrication process, SiC wafers are bonded to a Si/SiO_2 substrate and are then thinned by mechanical grinding and polishing, resulting in severe total thickness variation (TTV) of the SiC—around 2−5 μm across a 100 mm wafer.[7] Photonic components, such as grating couplers for input/output of light and microring resonators for frequency conversion, have strict requirements on the effective index and therefore SiC thickness to maintain the desired efficiency. Consequently, TTV is detrimental to performance and fabrication yield of photonic devices and limits the lateral dimension of optical elements. Wafer-scale production of photonic devices require <10 nm of TTV across the wafer to enable high fabrication yield and efficient coupling of optical elements. Instead of grinding and polishing, ion-cutting and layer transferring methods have been demonstrated to fabricate wafer-scale SiCOI films with low TTV (<10 nm), but the high energy ion bombardment results in lattice damage and hence poor optical performance.[8−10] Additionally, defects created from ion bombardment will interfere with optical properties of color centers, and therefore, ion-cutting is generally considered to be incompatible with integrated quantum defects. In diamond, overgrowth after implantation has been shown to mitigate issues with lattice damage;[11] however, growth temperatures (>1600 °C) are not compatible with SiCOI device stacks due to the mismatch in the coefficients of thermal

Received: September 24, 2024
Revised: April 24, 2025
Accepted: April 24, 2025

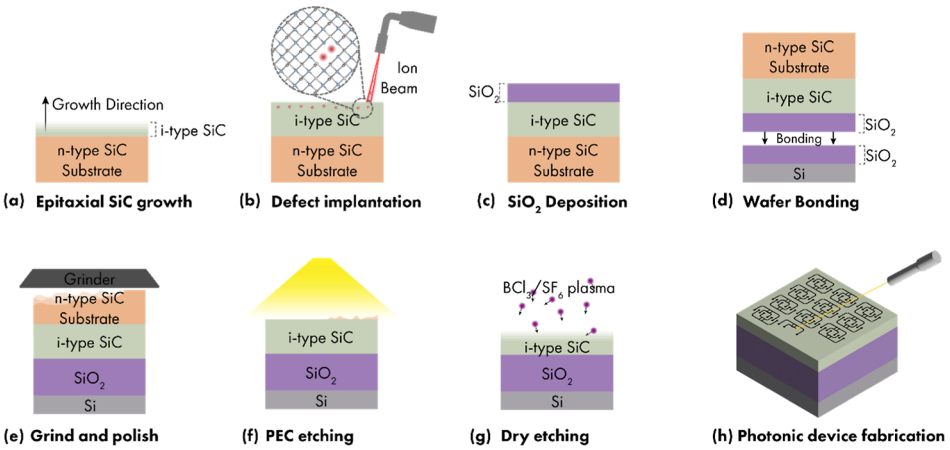


Figure 1. SiCOI fabrication process schematic depicting step-by-step process flow of SiCOI photonic device fabrication. (a) i-type SiC layer grown on the n-type substrate. (b) C ion implantation and anneal for formation of divacancy defect color centers near the SiC surface. (c) ICPCVD deposition of SiO_2. (d) Bonding of material stack in (c) to a Si/SiO_2 handle wafer. (e) Thinning of n-type substrate from bulk wafer to ∼6−8 μm by grinding and polishing, introducing additional TTV. (f) Dopant-selective PEC etching for removal of a n-type substrate layer, reducing TTV. (g) SF_6/O_2 Dry etching to thin the material to optimal thickness for single-mode waveguides. (h) Electron beam lithography patterning and dry etching to fabricate racetrack resonators.

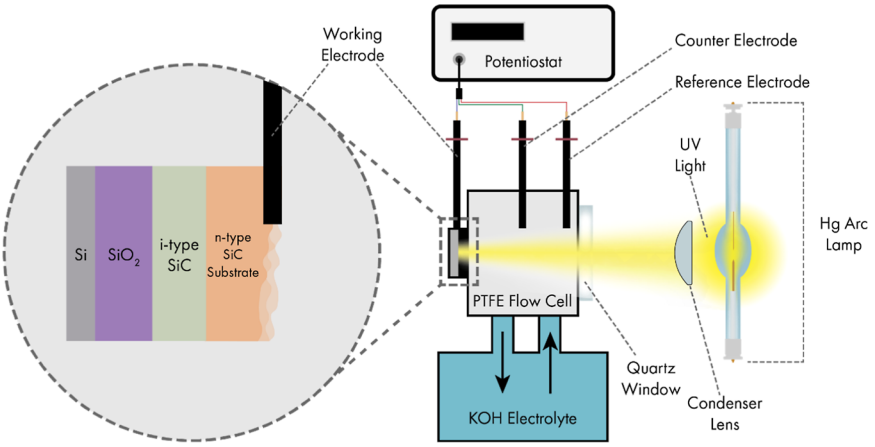


Figure 2. Experimental setup schematic of the three electrode photoelectrochemical flow cell with the SiC stack from Figure 1e as the working electrode, a Pt counter electrode, a Ag/AgCl reference electrode, and focused UV illumination.

expansion of SiO_2 and SiC. Thus, a SiCOI fabrication method which preserves the optical quality needed for quantum defects while also producing low TTV across a wafer has yet to be demonstrated. Selective wet etching with a sacrificial surface layer avoids the lattice damage associated with ion cutting, while eliminating the thickness variation associated with grinding and polishing.[2] Photoelectrochemical (PEC) etching is one of the few wet etching methods effective on SiC, and recent work has demonstrated smooth, dopant-selective etching of 4H−SiC layers using PEC etching in dilute KOH, which, when used with multiple etch stops, has sufficient selectivity to reduce TTV by 2 orders of magnitude.[12−15]

Here, we demonstrate the use of dopant-selective PEC etching for TTV reduction in SiCOI films by making use of a sacrificial n-type layer on top of an unintentionally doped (i-type) device layer. Using PEC etching after an initial grind and polish step (Figure 1), a SICOI film was fabricated with TTV of only 88 nm across a 1 cm diameter etched area, compared to 628 nm for our standard grind and polish technique (7× improvement). The improved thickness uniformity of our PEC-etched samples resulted in a higher yield of racetrack resonator devices that match the designed resonance and line width, compared to grind and polish samples. Further, SiCOI waveguides with divacancy defects were fabricated, and the PEC etching process was shown not to obfuscate zero phonon line (ZPL) emission. This work is one of the first to discuss the chip-to wafer-scale manufacturability of 4H−SiCOI and the results presented herein provide a significant step toward maturing the photonic platform.

RESULTS AND DISCUSSION

4H−SiCOI films schematically illustrated in Figure 1e were characterized for oxidation rate as a function of voltage under UV illumination using the PEC etching setup depicted schematically in Figure 2. The n-type sacrificial layer with a high thickness variation was etched first (Figure 3a, orange curve). The passivation peak voltage was found to be 0.97 V vs Ag/AgCl, so an etching voltage of 0.7 V vs Ag/AgCl was chosen to selectively etch the sacrificial layer (Figures 3b and S2). The choice of etching voltage is important; voltage chosen too low can result in low selectivity to the etch-stop layer, and voltage too high can result in unstable etching or premature passivation. The etching current was stable at ∼12 mA until the thinnest part of the n-type layer was fully etched (∼20 C),

https://doi.org/10.1021/acsphotonics.4c01834
ACS Photonics XXXX, XXX, XXX−XXX

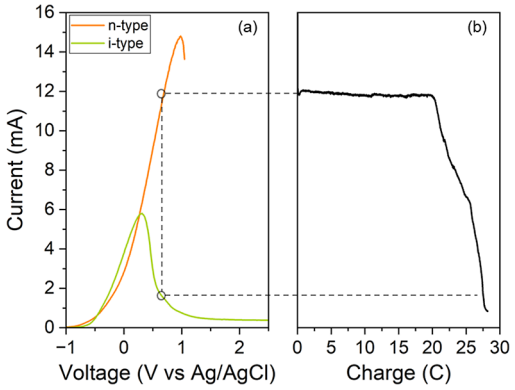


Figure 3. Electrochemical data (a) linear sweep voltammetry (LSV) curves of n-type (orange) and i-type (green) before and after performing selective PEC etch, respectively. (b) Constant voltage hold performed at 0.7 V vs Ag/AgCl and stopped once current stabilized after reduction due to selectivity.

at which point the current reduced as a result of the lower etch rate of the i-type layer at 0.7 V vs Ag/AgCl. Finally, after 29 C of charge had passed, the current stabilized at 0.8 mA (Figure S2), indicating that all of the n-type SiC had been etched away.

After stabilization of the etching current, an LSV sweep was performed to characterize the relative oxidation rates with respect to voltage of the i-type layer compared to that of the n-type sacrificial layer (Figure 3a). The i-type layer exposed by PEC etching passivates at a significantly lower voltage than the more highly doped n-type, consistent with previous reports by Pavunny et al.[16] The chosen etching voltage (0.7 V vs Ag/AgCl) is at more positive voltage than the passivation peak voltage in the i-type layer, resulting in a significantly decreased etch rate of the i-type compared to n-type, and hence good selectivity.

The gradual reduction in current from 20 to 29 C of transferred charge (1750 to 2750 s in Figure S2) is a result of the thickness variation in the n-type SiC. As the i-type layer is exposed, the average areal etch rate decreases, leading to a downward slope which is gradual if TTV of the layer is high. Using the ratios of etching current in the n-type layer vs the i-type layer as a ratio of etch rates, the selectivity of the PEC etch was estimated to be 15:1. Reduction in TTV can be observed visually by near elimination or rainbow-like interference patterns within etched area (Figure S3).

Characterization of the morphology of the SiC after PEC etching by cross-sectional SEM is depicted in etched vs unetched areas in Figure 4a,b, respectively. Secondary electron yield gives doping-dependent regions of darker and lighter contrast, enabling facile inspection of differently doped SiC. We observe distinct epitaxial layers, with the lower i-type layer thickness ~5.2 μm, the n-type buffer region thickness ~0.5 μm, and the n-type sacrificial layer ~3.8 μm. We note that due to the polishing-induced TTV, the thickness of the n-type sacrificial layer can vary by more than 1 μm depending on location. Clearly, the top n-type sacrificial layer and the n-type epitaxial buffer layer have been completely removed after PEC etching, with a minimal change in thickness of the i-type layer, demonstrating good selectivity (Figure 4c). The resulting etched area has low surface roughness (R_{rms} = 0.73 nm Figure S4). The ~5.5 μm etch depth characterized by stylus profilometry is consistent with the removal of the surface n-type layer and stoppage of the i-type layer below (Figure 4c).

To characterize the impact of dopant-selective PEC etching on TTV reduction, thickness mapping measurements were made on SiC samples at three stages of the fabrication process

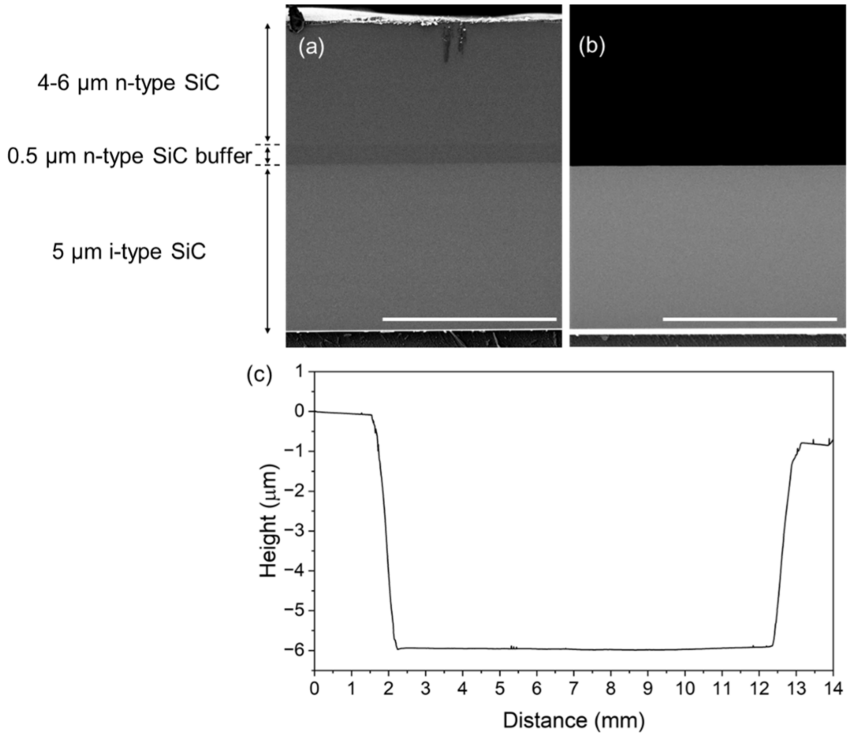


Figure 4. Etched material characterization cross-sectional SEM image of epitaxial SiC layers in SiCOI stack (a) after grind and polish and (b) after PEC etching. Scale bar is 5 μm. (c) Stylus profilometry characterization of etch depth and surface morphology following PEC etching.

https://doi.org/10.1021/acsphotonics.4c01834
ACS Photonics XXXX, XXX, XXX−XXX

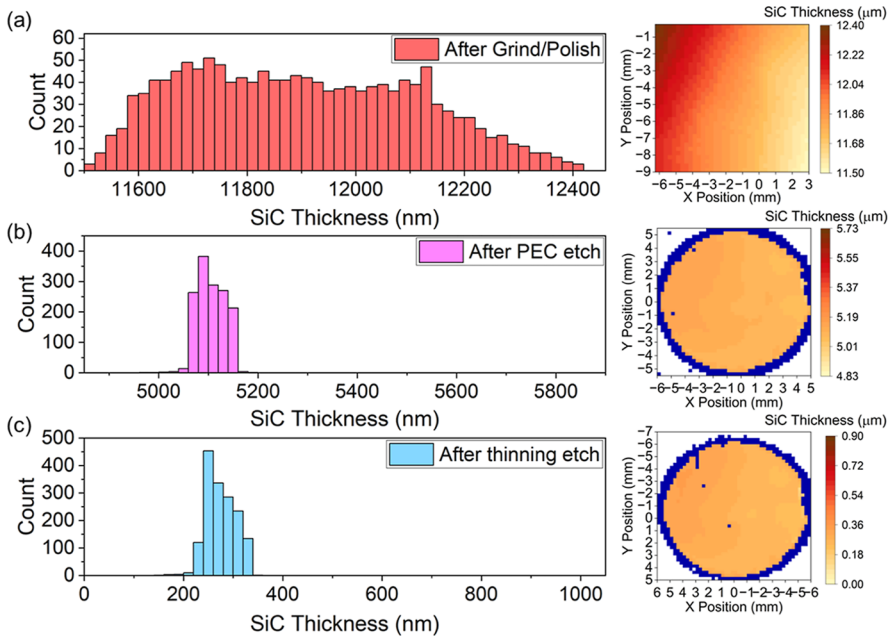


Figure 5. TTV analysis Thickness distributions and mapping for SiCOI samples (a) after grind and polish (b) after dopant-selective PEC etching and (c) after thinning to 250 nm. All areas measured for thickness are 0.79 mm^2.

outlined in Figure 1c–e; after the grind and polish (Figure 5a), after PEC etching (Figure 5b), and after thinning via dry etch to optimal photonic thickness (Figure 5c). All SiC areas compared for TTV were 79 mm^2, and measurements were made with a spacing of 0.25 × 0.25 mm. TTV is quantified by taking three standard deviations from the mean of the thickness measurements (3σ). After the grinding and polish step, the TTV is found to be 628 nm (Figure 5a). After PEC etching, the distribution of thicknesses is significantly narrower, with a measured TTV of 84 nm. This represents a factor of 7.5 lower TTV achieved by the selective PEC etching method. Finally, after dry etching to 250 nm the TTV is measured to be 88 nm, thus dry etching the remaining 4.75 μm of SiC does not significantly add to the TTV.

The thickness variation pattern apparent in the thickness map after grinding and polish has features over long (centimeter-scale) length scales, not uncommon in SiCOI films processed with this method. However, while the thickness differences are smaller, the thickness variation pattern after PEC etching has more intricate features (mm-scale). We expect that the thickness variation patterns present in the PEC etched samples are a result of the light intensity differences across the spot from the focused Hg lamp. To illustrate this, intensity profiles of the beam are compared with thickness maps and photographs of the PEC-etched SiC samples (Figure S5). Clearly, the light intensity pattern has transferred to the resultant thickness variation in the PEC etched samples. Thus, there is clearly a light-dependent etch rate, resulting in thickness variation being introduced to the etch stop, while thicker portions of the n-type sacrificial layer are still being removed.

Additionally, here we have demonstrated only TTV reduction using one etch stop, which also serves as the layer hosting photonic devices (discussed below). However, prior work has shown that using a greater doping contrast (i.e., p-type rather than i-type) results in improved selectivity[16] and stacking of multiple etch stops results in greater effective TTV reduction through multiple selective etches.[12] Photonic devices typically suffer higher propagation loss in layers with high doping, but in an optimized sacrificial multilayered stack, intermediate etch stop layers could be p-type while the final device layer remains i-type. Therefore, while the reduction in TTV demonstrated here is dramatic, there is further opportunity to improve TTV through improvement of light source uniformity, greater contrast between dopants, and multilayer stacking of contrasting dopant layers. We expect that making these simple changes to optimize the fundamental process outlined here would result in reaching the target <10 nm TTV across a 100 mm wafer."

To demonstrate that the PEC etching approach enables low-loss photonics with a high fabrication yield, we fabricated racetrack resonators after thinning to 250 nm. We fabricated 104 racetrack resonators with varied coupling lengths (14.53, 36.48, 46.67, and 55.35 μm) and found that 58% of these devices exhibit resonance and line widths matching our design, as compared to 19% of similar devices prepared on a chip without PEC etching (Figure S6 and Table S2). We chose to focus on the devices with the shortest coupling length (14.53 μm) since they exhibited the strongest resonances. Simulation results determining the optimal coupling length for a given propagation loss are shown in Figure S7. Thus, we chose to focus our analysis on these devices. Of these, clear resonances were observed in 100% of the devices contained within the PEC etched area. When the grind and polish method alone is used, we observe that less than half of our racetrack resonators exhibit clear resonances.

In 12 of 22 racetrack resonators tested, only one family of resonances were observed in the through and drop port spectra, indicating the desired single mode behavior. However, 10 of the devices exhibited more than one family of resonances, as indicated by the distinct sets of free spectral ranges (FSRs, Figure S8). We suspect that this multimode behavior is due to mode conversion in the device, possibly a result of TTV along the length of the waveguides since our grating couplers are optimized for transverse electric (TE)

https://doi.org/10.1021/acsphotonics.4c01834
ACS Photonics XXXX, XXX, XXX−XXX

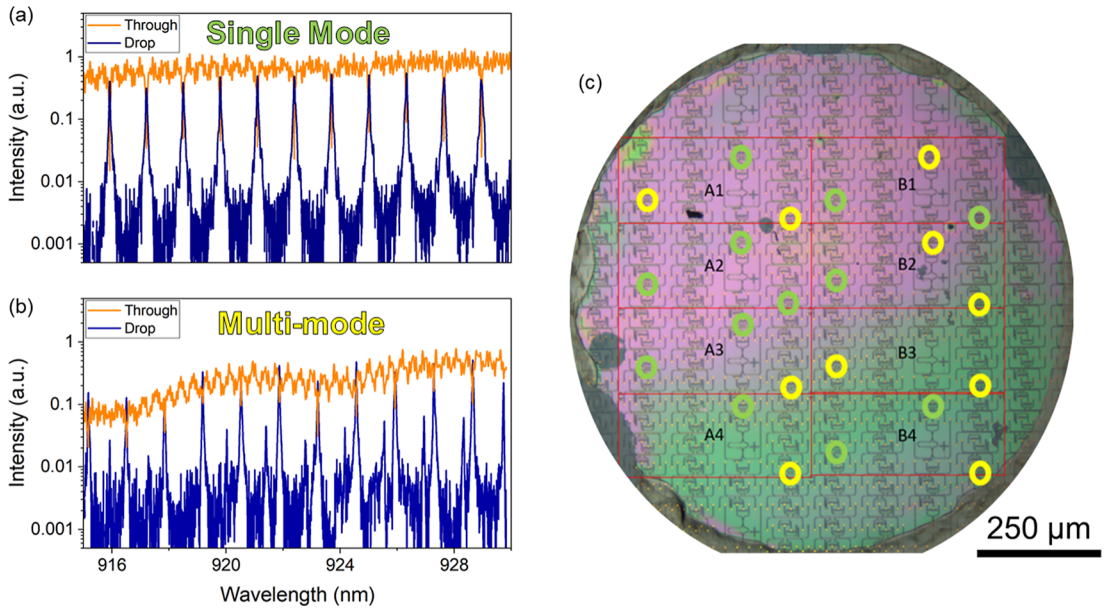


Figure 6. Optical testing overlaid through port and drop port spectra for racetrack resonators with circumference 201.7 μm exhibiting (a) TE family resonance modes and (b) a mix between TE and TM resonance modes as a result of thickness variation across the sample. (c) Map of optical elements on sample with single peak and split peak device locations differentiated via color.

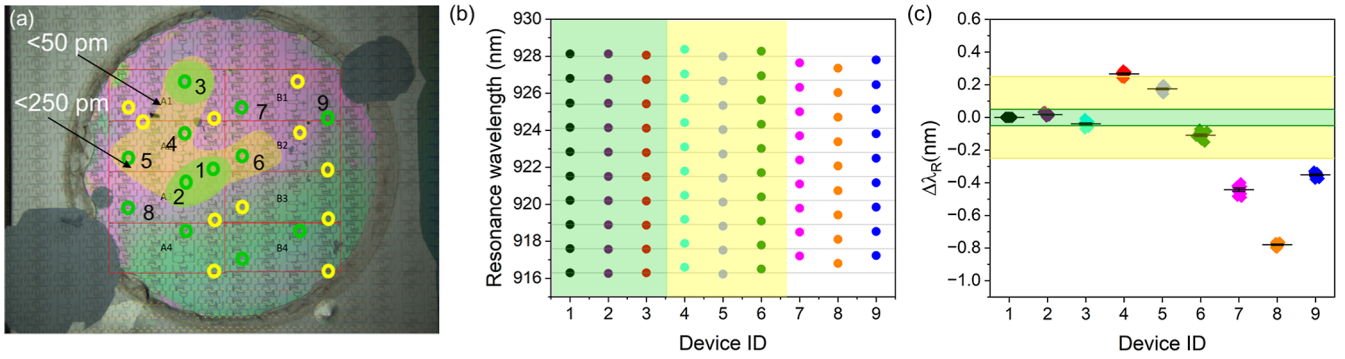


Figure 7. Resonance shifts. (a) Map of devices labeled 1−9 compared for resonant wavelength shifts. Devices within 50 pm of device 1 are contained in the green area, and devices within 250 pm are within the yellow area. (b) Plot of resonant wavelengths measured from through port of racetrack resonator and (c) deviation of resonant wavelength ($\Delta\lambda_R$) for devices mapped in (a). $\Delta\lambda_R$ is calculated in with respect to device 1. Peak position determined by Lorentzian fitting.

polarization and our waveguides support only a fundamental TE and transverse magnetic (TM) mode.

Of the single mode devices measured, the average propagation loss was 17 dB cm^{-1}. The best performing device was measured to have 2.2 dB cm^{-1}propagation loss, the lowest value reported for a single mode waveguide in SiCOI that the authors are aware of (Figure S9).[17] The champion resonator exhibits a loaded Q factor of 20,100. Based on the relation in eq 1, we extract an intrinsic Q factor, Q_i = 100,000, where n_g is the group index and α is the propagation loss. A Q-factor of 10^5 is a high value for single mode resonators in SiCOI at 920 nm, directly a result of the low propagation loss.[9,18,19]

$$Q_i = \frac{2\pi n_g}{\alpha \lambda_0} \tag{1}$$

Although TTV reduction could play a role in reducing the average propagation losses of waveguides across a chip (for example, reduction of mode conversion losses), it is also possible that the uniformity of the SiC material quality could play a role. We note a bulk value for SiC propagation loss at 1550 nm is < 0.1 dB/cm, though we are measuring at 920 nm in a confined medium, where scattering due to sidewall roughness becomes prevalent. We suspect that sidewall roughness (Rayleigh scattering) on our waveguides is currently limiting our propagation loss, an aspect which we have not yet attempted to optimize.

The location of devices on the chip exhibiting single mode or multimode resonance is shown in Figure 6c with single mode devices depicted as green circles and multimode devices depicted as yellow circles. Interference patterns on the microscope image are present in SiCOI films as a result of contrasting refractive index of the underlying oxide, allowing for visual indication of thickness (Figure S4). The areas of the chip that appear green in color to the eye are thicker than the areas that appear pink, with thicknesses ∼310 vs ∼260 nm, respectively (Figure S10). Thus, we can see that a greater fraction (70%) of the devices in the thinner part of the chip appear to be single mode resonators, as compared to 33% in the thicker green region. Clearly, a significant fraction of the devices perform with high quality, but there is still room for

https://doi.org/10.1021/acsphotonics.4c01834
ACS Photonics XXXX, XXX, XXX−XXX

improvement. These results reinforce the importance of TTV as a feature of SiCOI device fabrication which needs additional attention in order for realization of 4H−SiCOI photonics at large scale.

In a wafer-scale photonic platform, it is not only necessary to fabricate a high yield of single-mode devices but also important that all devices are functionally identical across the chip. Since the effective index of a guided mode is dependent upon the geometry of the waveguide and hence the thickness of the SiC layer, resonant wavelengths of our devices are thickness dependent. One way to compensate for deviations of the resonant wavelengths due to TTV is to use the electro-optic effect intrinsic to SiC. We estimate that electro-optical tuning can shift resonant wavelength with a voltage of ∼1 pm/V.[20,21] Thus, as an estimate, a 50 pm (∼50 V) shift should be within the dielectric breakdown window, and a 250 pm (250 V) shift could potentially be accessible.

The nine devices exhibiting single mode resonance in the thinner (pink) region of the chip are labeled with identifiers in Figure 7a. The resonant peak wavelengths are plotted for each device in Figure 7b, and the difference between peaks of a given mode is calculated as $\Delta\lambda_R$ in Figure 7c. It was found that devices 1−4 are within the 50 pm range for electro-optic tuning, and devices 5 and 6 are within 250 pm. Devices 7−9 are all deviating from Device 1 by > 250 pm, and therefore by our estimation are not within range of electro-optic tuning. Further, the standard deviation of the loaded Q factors of these devices is roughly 10% of the average, indicating that the geometry and dimensions of the racetrack resonators are similar (Figure S11). The proximity of the functioning devices within an area of a relatively constant thickness is further illustration of the importance of low TTV for production of scalable SiCOI photonics. The ability to make 3 nearly identical SiC racetrack resonators spaced by > 5 mm is illustrative of the impact the selective PEC etching method has on manufacturability of SiCOI photonics.

In order to be useful in quantum technologies, it is critical that all SiCOI fabrication processes do not interfere with the optical emission of quantum color centers. To demonstrate that the PEC etching process is compatible with maintaining high quality color center emission, SiC wafers were implanted with divacancy defects prior to SiO_2 deposition (Figure 1b) and then carried through the remainder of the process steps, including PEC etching. Waveguides are fabricated with features optimized for detecting ZPL emission (Figures 8 and S12); the waveguide has grating couplers on one side tuned to 920 nm (corresponding to the off-resonant excitation used herein), and the other side to 1107 nm (corresponding with the PL3 *kh* basally oriented divacancy defect ZPL).[4,22] The waveguides are single mode for ZPL emission, and with randomly distributed defects in the waveguide, the coupling of defect emission into the waveguide is not known. After cooling to 7 K, we detected a strong ZPL emission from the output grating coupler, with the most intense peak being the PL3 emission, corresponding to the design of our grating coupler. Although PL4 (basally oriented *hk* divacancy defect) should couple well to a TE waveguide mode, the ZPL intensity here is relatively weak most likely due to the limited bandwidth of the grating coupler. Similarly, PL5 and PL6 both lie far below the optimized wavelength of our grating couplers, centered at 1107 nm, and are thus not observed. On the other hand, the ZPLs of PL1 and PL2 (axially oriented *hh* and *kk* defects, respectively) appear as broad, weak features, which we speculate is due to their preferred coupling with a TM waveguide mode. Thus, unlike ion-cutting methods to reduce TTV, PEC etching does not prevent strong emission of color centers and, as such, is one of the only methods to produce low-TTV SiCOI with compatibility for waveguide-integrated color centers.

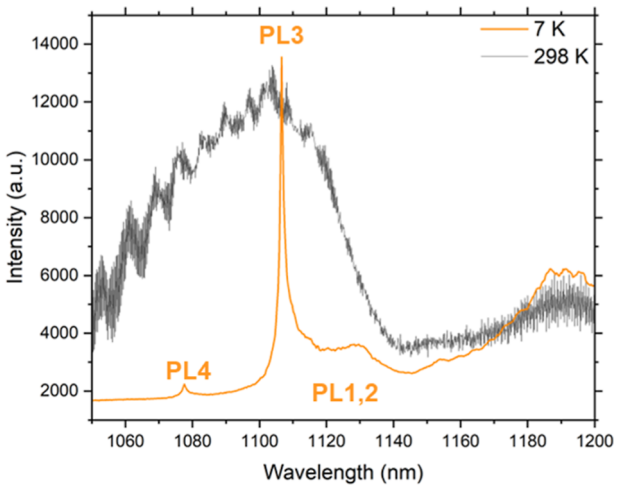


Figure 8. ZPL emission measurement emission spectra from the output of waveguide-integrated defects at 298 K and 7 K. Upon cooling, sharp ZPLs emerge for basally oriented PL3 and PL4, and broad features for axially oriented PL1 and PL2.

CONCLUSIONS

Here, we have demonstrated an approach to improving the feasibility of 4H−SiCOI as a quantum photonic platform by fabricating SiCOI films with low TTV via dopant-selective PEC etching. Racetrack resonators on SiCOI films fabricated using the selective PEC etching method had a low average and champion propagation loss (17 dB/cm, 2.2 dB/cm), and a 58% yield of high-quality single mode resonators within a 0.8 cm^2 area. Resonant modes of several resonators are within range of electro-optic tuning, enabling fabrication of functionally identical devices across mm-scale distances. SiCOI implanted with divacancy defects exhibit strong ZPL emission at 1107 nm, demonstrating compatibility with waveguide-integrated quantum color centers. This work is one of the first to evaluate fabrication yield, quality, and resonance variation of multiple optical elements on chip in 4H−SiCOI, clearly demonstrating the challenges faced in maturing the 4H−SiCOI technology. Despite the challenges, our results herein suggest that PEC can provide a viable path forward for SiCOI technologies, with a path to <10 nm TTV across a wafer. Such a dramatic improvement in SiC thin film uniformity would provide unprecedented opportunities for SiCOI photonics.

EXPERIMENTAL METHODS

SiCOI Fabrication. Monocrystalline samples for PEC etching consisted of commercial n-type 4H−SiC substrates (4° off-axis, resistivity 0.015−0.028 Ω cm, 100 mm diameter, 350 μm thick). Epitaxy began on the C-face with 0.5 μm thick n-type buffer layer ($[N] \geq 5 \times 10^{18}$ cm^{-3}), followed by a 5 μm unintentionally doped (i-type) layer ($[N] = 1 \times 10^{14}$ cm^{-3}, Figure 1a). Five μm thickness is used as the etch stop thickness to allow sufficient UV absorption for PEC etching. Substrates with grown C-face epitaxial layers were obtained from STMicroelectronics.

https://doi.org/10.1021/acsphotonics.4c01834
ACS Photonics XXXX, XXX, XXX−XXX

Wafers were initially cleaned with Piranha (H_2SO_4/H_2O_2 4:1) and downstream plasma washing to remove organics. Samples with divacancy defects were implanted with carbon ions at a dose of 5×10^{11} and annealed at 850 °C for 1 h. A few μm layer of SiO_2 was deposited by ICPCVD on the surface of the i-type layer, followed by anneal to densify the SiO_2. Chemical mechanical polishing is then performed on SiO_2 to render a desired thickness for device fabrication and a suitable surface finish for bonding (Figure 1c). The wafer is then bonded such that the top SiO_2 layer is bonded to the SiO_2 on an Si/SiO_2 handle wafer by annealing at 200 °C for 3 days (Figure 1d). This structure exposed the Si face. Following bonding, mechanical grinding and polishing was performed to reduce the thickness of the n-type substrate to 6−8 μm (Figure 1e). Ohmic contacts were patterned with photolithography, and the exposed SiC surface was treated with an O_2-plasma descum and close-coupled dilute ∼1 wt % % HF for 1 min to remove organic residues and native oxide, respectively. This was followed by e-beam evaporation of 100 nm thick Ni ohmic contacts and metal liftoff. Samples were diced into 20 mm × 20 mm squares containing 20 mm × 3 mm strips of Ni on two sides. Ohmic contacts were activated by rapid thermal annealing at 950 °C in Ar for 2 min. Typical resistance across the 2 contacts on the SiCOI film before PEC etching was <30 Ω.

Photoelectrochemical Etching. Photoelectrochemical etching was performed on the samples described above using a custom photoelectrochemical cell (Figure 2) with a Solartron SI 1287 potentiostat. Additional experimental details about cell dimensions, electrical contact application, and temperature/flow parameters can be found in our previous work.[12] The SiC sample working electrode was inserted into the cell such that the Si face surface was exposed to flowing KOH (1 wt %/0.18 M) in a flat cell configuration with a platinum wire counter electrode and a Ag/AgCl reference electrode. Electrolyte was circulated to maintain a constant temperature during illumination and provide perturbation for dissolution of oxidation products. All electrochemical experiments were performed at room temperature (∼21 °C). A Hamamatsu LC8 Hg−Xe lamp was used as the light source, and an aspheric condenser lens was used to focus the light onto the sample. The light intensity through the aperture of the electrochemical cell was measured to be 3.5 W cm^{-2} using a S310C thermal power surface absorber at a wavelength of 365 nm.

LSV and chromatoamperometry (CA) were used to characterize the voltage-dependent oxidation rate and perform a constant voltage etch, respectively. n-type SiC is stable in 1% KOH with no visible etching at open circuit and little dark current in the relevant voltage window (−1 to 3 V vs Ag/AgCl). In a typical LSV experiment, the applied voltage was swept to positive (anodic) voltages, and the resulting current is used to determine oxidation rate. Anodic sweeps were stopped just after the crest of the passivation peaks to prevent passivation prior to the CA etching experiments. After the etching behavior was characterized with LSV, etching was performed at a fixed voltage, chosen to be more negative than the passivation peak voltage.

Etch Characterization. Following etching, samples were characterized by stylus profilometry (KLA Tencor Profiler) to determine depth. As a result of grinding and polishing, the surface of the SiC was not level, so further data processing was required to account for the discrepancies from the profiler's software. Briefly, parabolic fits were made to the unetched area and subtracted from the data set. The etched area was assumed to be flat relative to the depth of the etch (∼6 μm) based on ellipsometry mapping data and interference patterns. A linear fit of the unetched area was then subtracted from the etched area.

Atomic force microscopy (Bruker Dimension Fastscan) was used to characterize the surface roughness and morphology. Cross-sectional SEM was performed using a Hitachi S-4800 SEM. Ellipsometry mapping was performed using a Woollam RC2 Small Spot System. Spectroscopic data for ellipsometry were taken from 600 to 1500 nm with a distance of 0.25 mm between points and a spot size of 25 μm × 40 μm.

Fabrication of Photonic Devices. After the PEC etch, SF_6/O_2 reactive ion etching (RIE) was used to thin down the exposed i-type SiC layer further for photonic circuit fabrication with target thickness of 250 nm for the SiC thin film. Then, 500 A Al_2O_3 was deposited by ALD as a hard mask at 200 °C. ZEP resist was used to pattern photonic device through electron beam lithography. BCl_3/Cl_2 RIE was used to etch Al_2O_3, and SF_6/O_2 RIE was used to etch the SiC layer in the shape of photonic devices. After the SiC etch, the Al_2O_3 mask was removed by NH_4OH solution immersion for 40 min.

Optical Testing. Racetrack resonators were characterized on a waveguide test setup under ambient conditions. A schematic of the setup and resonator layout is shown in Figure S13. A tunable laser (Toptica CTL 950) was coupled into a fiber, sent through a polarization controller, and directed to a V-groove fiber array. Some of the input light was directed to a wavelength meter (Bristol 871A-NIR) and reference photodiode (Newport 2011-FC-M) via 99:1 fiber beam splitters. After transmission through a photonic waveguide device, light was collected by adjacent fibers in the V-groove array and directed to additional photodiodes. The voltage output from the photodiodes was readout by a DAQ (National Instruments USB-6356). Fiber alignment to the grating couplers is achieved through a series of XYZθ stages. Once the alignment was optimized, the polarization of light upstream in the fiber was adjusted to maximize transmission through a device on chip. The wavelength of the laser was then continuously tuned over the desired range while the transmitted power is simultaneously recorded by the DAQ. Propagation loss was extracted from the racetrack resonator data after applying a peak fitting algorithm and utilizing the analytical equations provided in Xia et al.[23]

Waveguides with divacancy defects were characterized in a Montana Cryostation s-100 instrument with a base temperature of 4 K (sample stage temperature of 7 K). The fiber setup described above was used to prepare off-resonant excitation light near 920 nm, delivered to photonic waveguides via a different V-groove array housed inside the Montana cryostat. The V-groove array was in a fixed position, and alignment to grating couplers was achieved with an Attocube XYZ stage configuration. The output from the waveguide with defects was directed into another fiber in the V-groove array, passed through a 950 nm long pass filter, and directed to a spectrometer (Princeton Instruments HRS-500, PyLoN IR).

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsphotonics.4c01834.

https://doi.org/10.1021/acsphotonics.4c01834
ACS Photonics XXXX, XXX, XXX−XXX

Additional description of the PEC etching mechanism, materials characterization of the etched samples, and supporting photonic device data (PDF)

AUTHOR INFORMATION

Corresponding Authors

Jason Lipton − *HRL Laboratories LLC, Malibu, California 90265, United States*; Email: jlipton@hrl.com

Shanying Cui − *HRL Laboratories LLC, Malibu, California 90265, United States*; orcid.org/0009-0001-7349-4510; Email: scui@hrl.com

Authors

Brett Yurash − *HRL Laboratories LLC, Malibu, California 90265, United States*

Adam Sorensen − *HRL Laboratories LLC, Malibu, California 90265, United States*

John Vajo − *HRL Laboratories LLC, Malibu, California 90265, United States*; orcid.org/0000-0002-6271-4899

Samuel Whiteley − *HRL Laboratories LLC, Malibu, California 90265, United States*

Tong Wang − *HRL Laboratories LLC, Malibu, California 90265, United States*

Biqin Huang − *HRL Laboratories LLC, Malibu, California 90265, United States*

Xiwei Bai − *HRL Laboratories LLC, Malibu, California 90265, United States*

Adrian Portales − *HRL Laboratories LLC, Malibu, California 90265, United States*

Sam Rubin − *HRL Laboratories LLC, Malibu, California 90265, United States*

Judas Strayer − *HRL Laboratories LLC, Malibu, California 90265, United States*

Jason Graetz − *HRL Laboratories LLC, Malibu, California 90265, United States*

Complete contact information is available at: https://pubs.acs.org/10.1021/acsphotonics.4c01834

Notes

The authors declare the following competing financial interest(s): J. L., B.Y., A.S., S.W., S.C., J.V., and J.G. are inventors on patents (granted and pending) related to this work.

ACKNOWLEDGMENTS

This work was supported by Boeing Disruptive Computing, Networks and Sensors, and is covered by United States Patents and Patents Pending. We thank John Lowell and Shuoqin Wang for helpful discussions, Russell Mott for assistance with the experimental setup, and Tommy Tran and Brendan Warren for help with sample fabrication. We thank Luke Quezada for assistance in making graphics.

REFERENCES

(1) Anderson, C. P.; Glen, E. O.; Zeledon, C.; Bourassa, A.; Jin, Y.; Zhu, Y.; Vorwerk, C.; Crook, A. L.; Abe, H.; Ul-Hassan, J.; Ohshima, T.; Son, N. T.; Galli, G.; Awschalom, D. D. Five-Second Coherence of a Single Spin with Single-Shot Readout in Silicon Carbide. *Sci. Adv.* **2022**, *8* (5), No. eabm5912.

(2) Crook, A. L.; Anderson, C. P.; Miao, K. C.; Bourassa, A.; Lee, H.; Bayliss, S. L.; Bracher, D. O.; Zhang, X.; Abe, H.; Ohshima, T.; Hu, E. L.; Awschalom, D. D. Purcell Enhancement of a Single Silicon Carbide Color Center with Coherent Spin Control. *Nano Lett.* **2020**, *20* (5), 3427−3434.

(3) Fang, R.-Z.; Lai, X.-Y.; Li, T.; Su, R.-Z.; Lu, B.-W.; Yang, C.-W.; Liu, R.-Z.; Qiao, Y.-K.; Li, C.; He, Z.-G.; Huang, J.; Li, H.; You, L.-X.; Huo, Y.-H.; Bao, X.-H.; Pan, J.-W. Experimental Generation of Spin-Photon Entanglement in Silicon Carbide. *Phys. Rev. Lett.* **2024**, *132* (16), 160801.

(4) Koehl, W. F.; Buckley, B. B.; Heremans, F. J.; Calusine, G.; Awschalom, D. D. Room Temperature Coherent Control of Defect Spin Qubits in Silicon Carbide. *Nature* **2011**, *479* (7371), 84−87.

(5) Lukin, D. M.; Guidry, M. A.; Yang, J.; Ghezellou, M.; Deb Mishra, S.; Abe, H.; Ohshima, T.; Ul-Hassan, J.; Vučković, J. Two-Emitter Multimode Cavity Quantum Electrodynamics in Thin-Film Silicon Carbide Photonics. *Phys. Rev. X* **2023**, *13* (1), 011005.

(6) Majety, S.; Saha, P.; Norman, V. A.; Radulaski, M. Quantum Information Processing with Integrated Silicon Carbide Photonics. *J. Appl. Phys.* **2022**, *131* (13), 130901.

(7) Lukin, D. M.; Dory, C.; Guidry, M. A.; Yang, K. Y.; Mishra, S. D.; Trivedi, R.; Radulaski, M.; Sun, S.; Vercruysse, D.; Ahn, G. H.; Vučković, J. 4H-Silicon-Carbide-on-Insulator for Integrated Quantum and Nonlinear Photonics. *Nat. Photonics* **2020**, *14* (5), 330−334.

(8) Yi, A.; Zheng, Y.; Huang, H.; Lin, J.; Yan, Y.; You, T.; Huang, K.; Zhang, S.; Shen, C.; Zhou, M.; Huang, W.; Zhang, J.; Zhou, S.; Ou, H.; Ou, X. Wafer-Scale 4H-Silicon Carbide-on-Insulator (4H−SiCOI) Platform for Nonlinear Integrated Optical Devices. *Opt. Mater.* **2020**, *107*, 109990.

(9) Zheng, Y.; Pu, M.; Yi, A.; Chang, B.; You, T.; Huang, K.; Kamel, A. N.; Henriksen, M. R.; Jørgensen, A. A.; Ou, X.; Ou, H. High-Quality Factor, High-Confinement Microring Resonators in 4H-Silicon Carbide-on-Insulator. *Opt. Express* **2019**, *27* (9), 13053.

(10) Wang, C.; Fang, Z.; Yi, A.; Yang, B.; Wang, Z.; Zhou, L.; Shen, C.; Zhu, Y.; Zhou, Y.; Bao, R.; Li, Z.; Chen, Y.; Huang, K.; Zhang, J.; Cheng, Y.; Ou, X. High-Q Microresonators on 4H-Silicon-Carbide-on-Insulator Platform for Nonlinear Photonics. *Light:Sci. Appl.* **2021**, *10* (1), 139.

(11) Piracha, A. H.; Ganesan, K.; Lau, D. W. M.; Stacey, A.; McGuinness, L. P.; Tomljenovic-Hanic, S.; Prawer, S. Scalable Fabrication of High-Quality, Ultra-Thin Single Crystal Diamond Membrane Windows. *Nanoscale* **2016**, *8* (12), 6860−6865.

(12) Whiteley, S.; Sorensen, A.; Vajo, J. J.; Sfadia, R.; Ladd, T. D.; Cui, S.; Graetz, J. Dopant Selective Photoelectrochemical Etching of SiC. *J. Electrochem. Soc.* **2023**, *170* (3), 036508.

(13) Whiteley, S.; Yap, D.; Chen, E.; Kim, D.; Ladd, T. D. Fabricating a silicon carbide and nitride structures on a carrier substrate. U.S. Patent 11,361,964 B2, 2020.

(14) Whiteley, S.; Yap, D.; Chen, E.; Kim, D.; Ladd, T. D. Silicon Carbide and Nitride Structures on a Substrate. U.S. Patent 11,714,231 B2, 2020.

(15) Whiteley, S.; Cui, S.; Graetz, J.; Vajo, J. J.; Sorensen, A. Forming a Planar Semiconductor Surface. U.S. Patent 2,024,042,9041 A1, 2024.

(16) Pavunny, S. P.; Myers-Ward, R. L.; Daniels, K. M.; Shi, W.; Sridhara, K.; DeJarld, M. T.; Boyd, A. K.; Kub, F. J.; Kohl, P. A.; Carter, S. G.; Gaskill, D. K. On the Doping Concentration Dependence and Dopant Selectivity of Photogenerated Carrier Assisted Etching of 4H−SiC Epilayers. *Electrochim. Acta* **2019**, *323*, 134778.

(17) Zhou, L.; Yi, A.; Su, Y.; Yang, B.; Zhu, Y.; Cai, J.; Wang, C.; Wu, Z.; Song, S.; Zhang, J.; Ou, X. High-Q Adiabatic Micro-Resonators on a Wafer-Scale Ion-Sliced 4H-Silicon Carbide-on-Insulator Platform. *Opt. Lett.* **2023**, *48* (23), 6279.

(18) Rabiei, P.; Steier, W. H.; Cheng, Z.; Dalton, L. R. Polymer Micro-Ring Filters and Modulators. *J. Lightwave Technol.* **2002**, *20* (11), 1968−1975.

(19) Guidry, M. A.; Yang, K. Y.; Lukin, D. M.; Markosyan, A.; Yang, J.; Fejer, M. M.; Vučković, J. Optical Parametric Oscillation in Silicon Carbide Nanophotonics. *Optica* **2020**, *7* (9), 1139.

(20) Fan, T.; Wu, X.; Vangapandu, S. R. M.; Hosseinnia, A. H.; Eftekhar, A. A.; Adibi, A. Racetrack Microresonator Based Electro-

Optic Phase Shifters on a 3C Silicon-Carbide-on-Insulator Platform. *Opt. Lett.* **2021**, *46* (9), 2135.
(21) Powell, K.; Li, L.; Shams-Ansari, A.; Wang, J.; Meng, D.; Sinclair, N.; Deng, J.; Lončar, M.; Yi, X. Integrated Silicon Carbide Electro-Optic Modulator. *Nat. Commun.* **2022**, *13* (1), 1851.
(22) Magnusson, B.; Son, N. T.; Csóré, A.; Gällström, A.; Ohshima, T.; Gali, A.; Ivanov, I. G. Excitation Properties of the Divacancy in 4 H -SiC. *Phys. Rev. B* **2018**, *98* (19), 195202.
(23) Xia, F.; Sekaric, L.; Vlasov, Y. A. Mode Conversion Losses in Silicon-on-Insulator Photonic Wire Based Racetrack Resonators. *Opt. Express* **2006**, *14* (9), 3872.

https://doi.org/10.1021/acsphotonics.4c01834
ACS Photonics XXXX, XXX, XXX−XXX