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Dopant Selective Photoelectrochemical Etching of SiC

Samuel Whiteley,[1] Adam Sorensen,[1] John J. Vajo,[1] Roy Sfadia,[1,2] Thaddeus D. Ladd,[1] Shanying Cui,[1] and Jason Graetz[1,z]

[1]*HRL Laboratories, LLC, Malibu, California 90265, United States of America*
[2]*Department of Physics, University of California, Santa Cruz, Santa Cruz, California 95064, United States of America*

Single crystalline 4H-SiC is a wide-gap semiconductor with optical properties that are poised to enable new applications in MEMS and quantum devices. A number of key hurdles remain with respect to the micro and nano-fabrication of SiC to prepare precise photonic structures with nanometer-scale precision. These challenges include development of a fast, scalable etching process for SiC capable of producing a sub-nanometer roughness semiconductor surface while simultaneously reducing the total thickness variation across a wafer. Our investigation into UV photoelectrochemical processing of SiC reveals high dopant-type selectivity and the advantage of multiple etch stops to reduce layer thickness variation. We demonstrate dopant-type selectivities >20:1 using a single step and a >100x reduction in surface variation by combining two etch stops. Moreover, the etch rate is fast (>4 μm h^{-1}) and the etched surface is smooth (~1 nm RMS). These results demonstrate a scalable path to the fabrication of precise nanoscale SiC structures and electronic devices that will enable the next generation of MEMS and photonic quantum devices.
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Wide band-gap semiconductors, including aluminum nitride (AlN), gallium nitride (GaN), and silicon carbide (SiC), are used in commercial devices such as micro-electromechanical systems (MEMS), and high-frequency and high-power electronics. 4H-SiC in particular has been shown to host defect centers as quantum memories in an integrated photonic platform,[1] and the ability to isotopically enhance the material makes the quantum memories in 4H-SiC more promising. Its nonlinear optical properties also suggest significant application potential for both quantum and classical photonics in clocking and wavelength transduction.[2,3]

Enabling the full application potential of these materials requires low-defect-density, uniform, wafer-scale thin-films of the material on insulator. However, neither Group III-Nitride nor hexagonal SiC can grow defect-free single crystals on common, low-cost substrates such as silicon due to lattice mismatches. While 3C-SiC grown on Si has hosted defect ensembles,[4–6] only homoepitaxial grown layers of SiC polytypes such as 4H-SiC have hosted isolated quantum memories with close to transform-limited optical linewidths.[7–10] Thin-film creation by traditional wet chemical etching techniques (aqueous acids, bases and molten salts) are ineffective in SiC,[11] as these lack sufficient etch rate selectivity, and further complicate the fabrication of both 4H-SiC and 6H-SiC devices. Current methods for fabricating optically and electrically isolated 4H-SiC on insulator (SiCOI) thin films either yield high lattice damage or have insufficient film thickness uniformity (total thickness variation, or TTV) across a wafer.[2,12] Wafer-scale production of linear[1] and nonlinear[3,13] photonic devices requires active layers with a TTV of <10 nm across the wafer to limit propagation loss with high device yield and to maintain high coupling efficiency to other optical elements. Reduction of TTV from ~1–2 μm, typical for low defect density mechanically polished and bonded SiCOI, down to <10 nm requires a wet etching process with a selectivity of $\gtrsim$ 100:1 between etch and etch-stop layers. Such selectivity is not offered by dry plasma etching techniques due to insufficient interlayer selectivity within SiC. Another etching process is required, which for practical manufacturing concerns should also be fast (>1 μm h^{-1}), wafer-scalable (>100 mm diameter substrates), and produce a smooth, non-porous surface (nm-scale roughness).

Photo-electrochemical (PEC) etching is one of the few room-temperature wet etching techniques with the potential for producing a wafer-scale, low-TTV, smooth, low-damage thin film of SiCOI and other materials.[14,15] This wet-etch technique avoids the high energy ions used in smart cut for SiCOI,[16] which has been shown to damage color centers in diamond,[17] impacting their quantum memory properties. PEC etching has the benefit of selectivity based on dopant-type and concentration.[18,19] This dopant selective etching has been used to fabricate undercut photonic structures by etching in-plane or laterally from recesses etched into the Si-face of SiC.[20,21]

We hypothesize that low TTV SiCOI can be prepared by photo-electrochemically etching down to an epitaxial defined dopant layer (which can also be the device layer) as shown in Fig. 1. A doped epitaxial layer therefore serves as an etch-stop. In this example, the base substrate is bulk 4H-SiC with an epitaxial sacrificial layer of doped 4H-SiC, followed by the relevant 4H-SiC layers necessary for the final device. Finally, a dielectric, such as silicon oxide (SiO_2), is deposited on top (Fig. 1a). The thickness range of epitaxial grown layers of SiC across a wafer can be well controlled to within <10% and we expect this to improve over time. This stack is wafer-bonded to a carrier substrate (handle wafer) such as Si/SiO_2 (Fig. 1b). In the next step the majority of the original SiC substrate is removed by mechanical grinding and polishing until the middle of the sacrificial layer is reached (Fig. 1c). Although the mechanical grinding and polishing can yield a locally smooth surface and uniform thickness over small length scales, ranging from micrometers to millimeters, the grinding usually yields non-uniform film thickness compared to a sub-micron thick target film across an entire wafer. Mechanical grinding may additionally introduce new lattice defects such as dislocations and crystal strain. Therefore, it is important to stop mechanical grinding in the *sacrificial* SiC layer (Fig. 1c) where this stopping layer is at least a few micrometers thick. The results presented here demonstrate that dopant selective PEC etching of the sacrificial layer(s) can reduce surface variations by >20 × for a single step (sacrificial *n*-type on a *p*-type etch stop layer) and by >100 × when two sacrificial layers are used to expose a clean, crystalline, low-defect-density, low TTV surface of SiC (Fig. 1d).

Electrochemical etching of SiC[18,22,23] occurs by a reaction between SiC, holes (h^+) located at the surface, and the electrolyte according to the reaction:[18]

$$SiC + 6h^+ + 8OH^- \rightarrow [Si(OH)_2O_2]^{2-} + CO + 3H_2O \qquad [1]$$

Alternatives include formation of insoluble products such as SiO_2 or $Si(OH)_2O$ or further oxidation of CO to CO_2 or CO_3^{2-}, which consume 8 h^+. The oxidation products are typically removed by

[z]E-mail: jagraetz@hrl.com

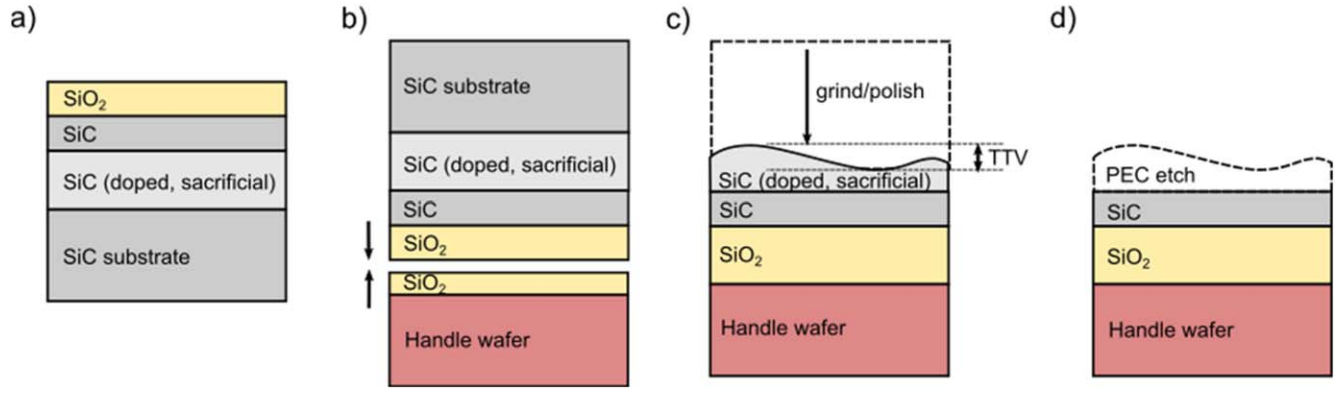

Figure 1. Method for fabricating high-quality, uniform thickness SiC on insulator. (a) SiC substrate with epitaxial-grown doped SiC sacrificial layer (e.g. *p*-type), followed by device SiC layer and an insulator SiO_2 deposited on top. (b) The original substrate is flipped and the SiO_2 layer is wafer-bonded to another substrate (handle wafer). (c) The SiC substrate that was used for epitaxial growth is thinned by mechanical grinding and chemical-mechanical polishing (CMP) resulting in a large TTV. (d) The sacrificial SiC layer, which was heavily doped, is selectively removed with photo-electrochemical etching to reduce/eliminate TTV of the SiC film. The illustration and respective material layer thicknesses are not drawn to scale.

dissolution into an electrolyte or gas evolution. In photoelectrochemical (PEC) etching, a UV light source with an energy greater than the bandgap (3.26 eV for SiC) is used to illuminate the near surface, producing electron-hole pairs that migrate to the semiconductor-electrolyte interface (space-charge region) under an applied potential bias. The rate of photoelectrochemical etching in SiC is dependent on a number of factors including the bias voltage, doping type and density, light intensity, electrolyte concentration and temperature. For *n*-type (N doped) SiC, band bending at this interface separates the electron-hole pairs and, with the appropriate bias, holes are confined to the surface leading to surface oxidation and etching. In *p*-type (Al doped) SiC, holes can be supplied from the bulk material in the absence of illumination or photogenerated as electron-hole pairs using UV light. Similar to *n*-type SiC, a bias voltage in *p*-type SiC is used to create band bending and thereby shuttle holes to or away from the surface. The differences in *n*- and *p*-type band bending behavior leads to dopant selectivity[24,25] where PEC etching occurs at lower bias voltages for *p*-type doping under illumination.[19] In addition, at sufficiently high voltages, the formation rate of etching (oxidation) products can exceed the rate of dissolution. This leads to passivation and a large decrease or cessation of etching.

In this work, we investigated dopant-selective PEC etching of Si-face SiC to better understand the limits of etching rates, surface roughness, and dopant level selectivity. Initially, we investigated a bulk N doped SiC to characterize the etch currents (as a function of bias potential) and determine the optimal etching conditions, we then characterized the etch rate and selectivity in a multilayer (*n–p–n*) SiC sample, and finally, we evaluated the effectiveness of dopant selective PEC etching on an artificially grooved sample to measure the surface variation reduction as a surrogate for TTV within the device layer. We demonstrated a wafer scalable PEC etching method capable of high rates ($>4\ \mu m\ h^{-1}$), producing uniform, smooth (nm-scale roughness) surfaces with a single layer dopant selectivity of >22:1 with much higher effective selectivities (180:1) possible by combining multiple alternating etch stop layers into a single stack.

Experimental Methods

Monocrystalline samples for PEC etch studies consisted of commercial *n*-type 4H-SiC substrates, which were 4° off-axis, low resistivity 0.015–0.028 Ohm-cm, 100 mm diameter, and 350 μm thick. The results discussed used material sourced by Wolfspeed Inc. (Cree Inc.). Additionally, we reproduced PEC etching on *n*-type bulk SiC (<0.03 Ohm-cm resistivity) substrates from STMicroelectronics Silicon Carbide and MSE Supplies, LLC. Epitaxy began with a 0.5 μm thick *n*-type buffer layer (N doped $5 \times 10^{18}\ cm^{-3}$) grown on the substrate, followed by 0.5 μm thick *p*-type (Al doped $7 \times 10^{18}\ cm^{-3}$) and 0.5 μm thick *n*-type (N doped $5 \times 10^{18}\ cm^{-3}$) layer growths.

Wafers were initially cleaned with Piranha (H_2SO_4:H_2O_2:H_2O 4:1:1) and downstream plasma washing to remove organics. On SiC wafers containing etched trenches for etch selectivity experiments, the trenches were lithographically defined using a photoresist mask, O_2 plasma descumed, and etched using an inductively coupled plasma (SF_6, Ar, O_2). Ohmic contacts were patterned with photolithography and the exposed SiC surface was treated with an O_2 plasma descum and close-coupled dilute ~5% wt HF (10:1 mixture of DI water:49% wt HF) for 1 min to remove organic residues and native oxide, respectively. This was followed by metal e-beam evaporation of 100 nm thick Ni for *n*-type ohmic contacts and metal liftoff. Samples were diced into 20 mm × 20 mm size squares containing 20 mm long × 3 mm wide strips of Ni on two edges. Rapid thermal processing was performed after dicing in order to allow for more flexibility over temperature studies and annealing methods. Ohmic contacts to the *n*-type were activated by a rapid thermal anneal (RTA) at 950 °C in argon for 2 min with a typical contact resistance of <1 Ω for the bulk material after annealing. To avoid diode-like behavior for the epitaxial *n–p–n* samples, contact to the *p*-type layer was made by partially exposing it, by scratching the surface, prior to Ni deposition.

Prior to PEC etching, each SiC sample was stripped of surface organic contaminants using Piranha etchant (4:1 mixture of 96% H_2SO_4 and 30% wt H_2O_2) for 2 min on the exposed SiC area between the ohmic contacts, followed by a deionized (DI) water rinse and drying.

Photoelectrochemical measurements.—Photoelectrochemical measurements were performed to characterize the rate of oxidation and surface etching as a function of bias voltage in a custom electrochemical cell shown in Fig. 2. Briefly, the SiC sample working electrode (1.3 cm^2 etched area) was immersed in an aqueous potassium hydroxide electrolyte (1 wt%/0.18 M) in a flat-cell configuration with a platinum wire counter electrode, and a Ag/AgCl reference electrode (all potentials reported herein are with respect to Ag/AgCl). Electrolyte was flowed through the cell to maintain a constant temperature during illumination. All electrochemical measurements were performed at room temperature (~21 °C) unless otherwise stated. The ultraviolet light was supplied by a Hamamatsu LC8 Mercury-xenon lamp with a −01A type 365 nm filter combined with an ultra-violet fused silica (UVFS) aspheric condenser lens (Edmund Optics 67–266). The light intensity at the PEC cell aperture was 3.5 W cm^{-2} measured with a 10 W

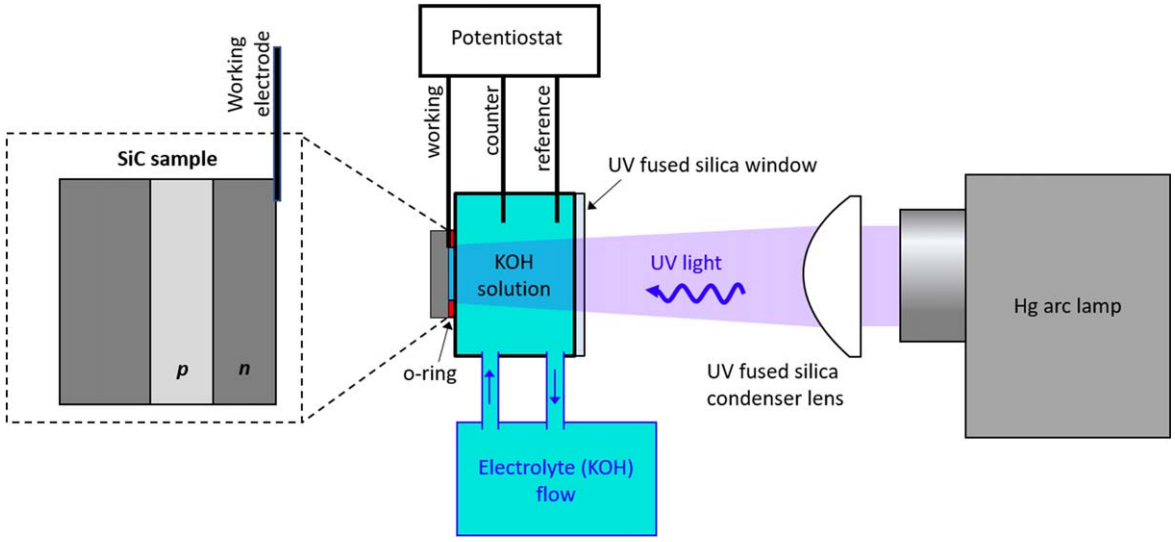

Figure 2. Schematic of three-electrode photoelectrochemical cell using a Pt counter electrode, a Ag/AgCl reference electrode and the doped SiC sample (working electrode) immersed in a flowing aqueous potassium hydroxide electrolyte (1 wt%/0.18 M) illuminated by an ultraviolet light (Mercury-xenon) fitted with a −01A type 365 nm filter and condenser lens converging the majority of the UV light within a 1.27 cm diameter aperture (1.3 cm^2).

S310C thermal power surface absorber sensor at a wavelength of 365 nm. Additional information regarding the photoelectrochemical cell and set-up is given in the supplementary information.

Linear sweep voltammetry (LSV) and chronoamperometry (CA) were used to characterize the electrochemical and PEC processes occurring on the SiC surface at various potentials. SiC is chemically stable in 1 wt% KOH with no etching at open circuit (chemical etch) and little-to-no dark current (electrochemical etch) expected when biased within a relevant potential window (e.g. −1 to 3 V). In a typical LSV measurement, the applied voltage was swept to positive (anodic) potentials and the resulting current used to determine the rate of oxidation (positive current). Anodic sweep measurements were stopped just after passivation peaks to avoid significant build-up of oxidation products thereby enabling subsequent CA measurements at chosen constant potentials. If needed to remove significant surface passivation, a cathodic sweep was performed. In extreme cases, the sample was removed and the passivation removed by etching with 5 wt% HF. It is worth noting that although LSV can be used to identify a particular reaction and estimate its potential, these measurements are made under dynamic potentials and provide limited information as to how a particular reaction (at a constant potential) changes over time. Insights into the reaction kinetics/dynamics are gleaned through CA. After characterizing the etching behavior with LSV, bulk etching was performed using CA at fixed potentials chosen from the LSV data.

Results and Discussion

PEC etching of n-type bulk SiC.—Initial PEC characterization measurements were performed on bulk *n*-type 4H-SiC using LSV acquired under an anodic sweep (−1.0 → 0.75 V), as shown in Fig. 3a. The current increased with the potential as expected, indicating SiC oxidation in reaction (1) and surface etching, reaching a peak of ∼14 mA at ∼0.70 V. Above this peak voltage (0.70 V) the surface passivated which led to a reduced current. An important practical consideration is that the LSV peak voltage and maximum current shift depending on the ohmic contact material, temperature of the electrolyte, incident light wavelength, incident light intensity (Fig. S1) and the manufacturer of the SiC.

As LSV scans do not reveal the etch dynamics, the doped SiC *n*-type bulk wafer was further etched using CA to determine the current stability and estimate etch rates at various bias potentials. Measurements were performed at nine different voltages relative to the passivation peak ranging from $\Delta V = -0.6$ V to +0.05 V with respect to the peak. An LSV scan was taken after each CA measurement to characterize the exposed surface's level of passivation. CA measurements (Fig. 3b) were performed until a total charge (integrated current) of 5C was transferred in order to reach similar etch depths. At all bias potentials, the initial current was equivalent to the value measured during the LSV sweep. At all potentials, up to and including the peak potential ($\Delta V = 0.00$ V), there was no passivation over the measurement window (5C). At higher potentials, above the oxidation peak ($\Delta V = +0.05$ V), the current fell off quickly and reached <2 mA after ∼20 s, suggesting rapid surface passivation. The *n*-type substrate CA experiments at multiple voltages demonstrates stable SiC etch rates in our PEC setup at working electrode voltage biases at and below the passivation peak potential. However, for different cell configurations and optics, CA performed near the passivation peak gave oscillating currents that eventually led to passivation as described in the Supplementary Information (Figs. S2, S3).

PEC etching from epitaxial n-type and p-type SiC.—We demonstrated dopant selective PEC etching on a SiC semiconductor consisting of an epitaxial grown *n*-type layer on top of a *p*-type layer. Figure 4a (blue curve) shows the LSV results on the surface *n*-type layer using an initial anodic sweep from −1.0 to 0.65 V. The increasing oxidation current reached a maximum of ∼11 mA at ∼0.55 V with a steep current drop at higher voltages indicating surface passivation. The *n*-type epitaxial layer's peak was similar to what was observed in the bulk *n*-type substrate (Fig. 3), but reached a current maximum at a lower potential (0.57 V as opposed to 0.70 V) and a lower current (∼11 mA as opposed to 14 mA). Note, the *n*-type epitaxial layers do not necessarily have the same dopant concentration and carrier density as the substrate. Continuous PEC etching was performed on the top *n*-type layer at a constant voltage of 0.47 V, which was ∼0.1 V below the oxidation peak ($\Delta V = -0.1$ V). This voltage was chosen to ensure uniform etching without the influence of passivation. The current measured during the PEC etch (Fig. 4b blue line) was consistent with the LSV results and relatively constant over the first ∼2.0C of charge transferred. After ∼2.5C the current decreased from ∼10 mA to 0.2 mA. This rapid drop in the oxidation current was associated with the transition from the *n*-type layer into the *p*-type layer.

After etching through the surface *n*-type layer, the underlying *p*-type layer was characterized using LSV to determine the relative oxidation (etching) potentials. The complete transition into the *p*-type layer was confirmed with a second LSV scan (solid red curve in

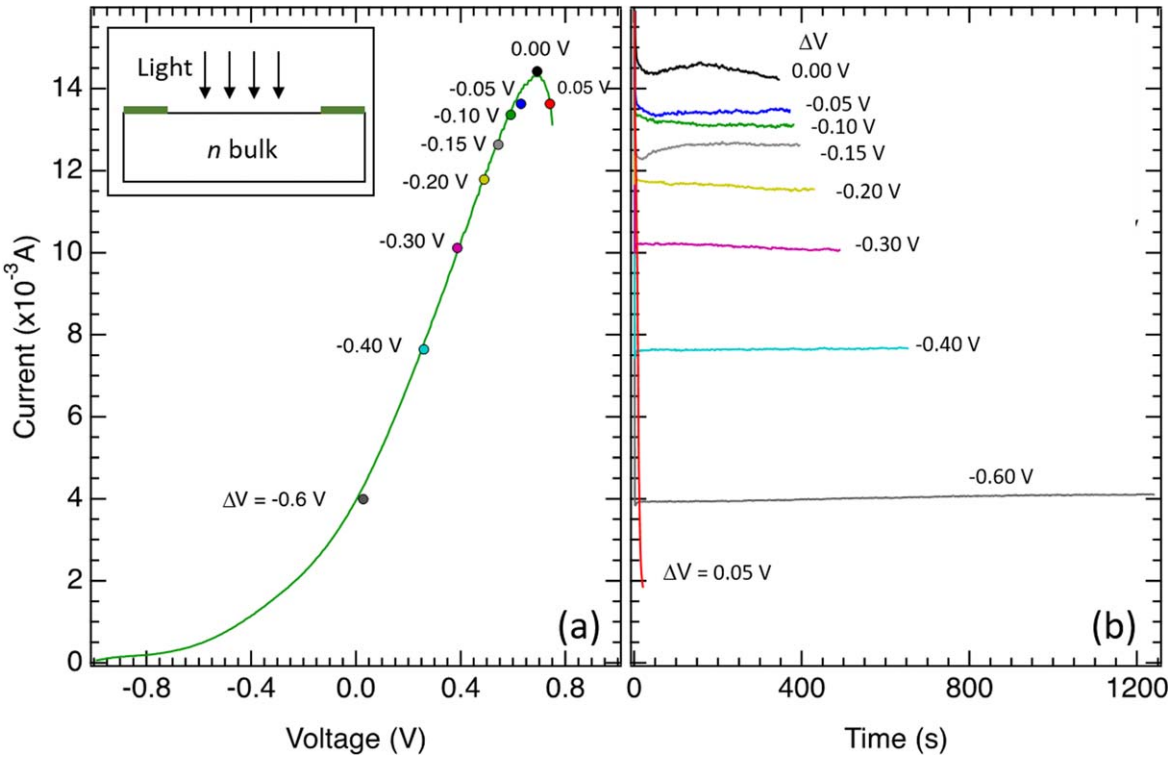

Figure 3. PEC etching of *n*-type bulk SiC. (a) Linear sweep voltammogram acquired under an anodic sweep (−1.0 → 0.75 V) on *n*-type bulk SiC (inset shows measurement configuration with contacts in green). (b) CA's performed at various bias voltages each for a total of 5C.

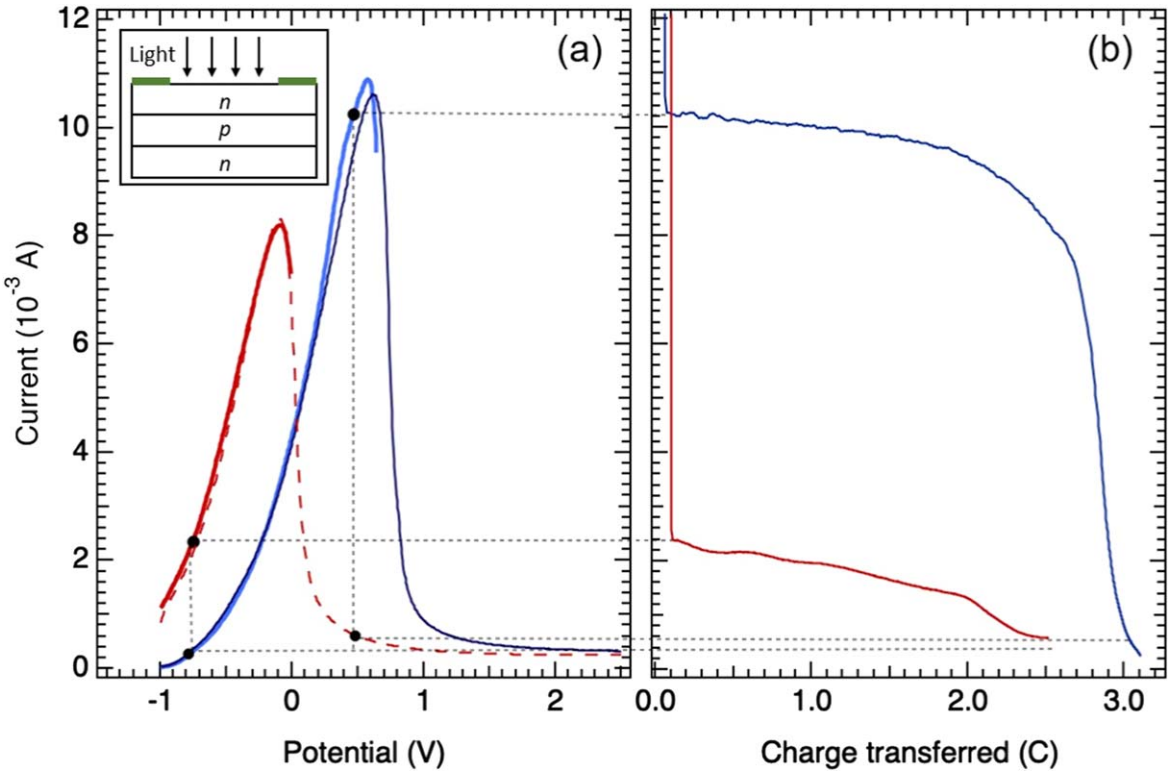

Figure 4. Selective PEC etching of an *n*-*p*-*n* layer stack. (a) LSVs from the top *n*-type surface layer (light blue), the underlying *p*-type layer (solid red) and the underlying *n*-type layer (dark blue), along with a full LSV from a *p*-type layer (dashed red) acquired from a different piece on the wafer. Black circles denote the voltage during CA etches and black dashed lines are guides to the eye for the expected currents. Inset shows the measurement configuration (contacts in green). (b) CA etching performed at 0.47 V (blue) showing etching of the top *n*-type layer through to the underlying *p*-type layer, and −0.75 V (red) showing etching of the *p*-type layer through to the underlying *n*-type layer.

Fig. 4a), which showed a passivation peak current at −0.1 V consistent with known lower etching potentials for *p*-type SiC under illumination.[19] To avoid excessive surface passivation, data collection for the *p*-type layer LSV was halted just past the oxidation peak. A full LSV measurement from −1.0 to 2.5 V in the *p*-type layer performed on a different piece of the wafer is also shown in Fig. 4a (dashed red line). In the absence of light, the flat band potentials in p-type SiC suggest the onset of oxidation (etching) should occur at ∼1.25 V, which is ∼2 V higher than the expected n-type onset and consistent with previous dark current measurements.[18,22] However, in the light, the band bending of both n- and p-type SiC change and the onset of etching in p-type shifts to a much more negative potential creating a condition where the onset of p-type etching occurs at a similar (or even slightly lower potential) than n-type, as previously observed by Pavunny et al.[19]

The *n*:*p* etch rate selectivity was determined using the ratio of CA currents measured during the transition from the *n*-type into the *p*-type layer. At 0.47 V, the etching potential was near (slightly below) the n-type passivation peak, but significantly above (+0.57 V) the *p*-type passivation peak. Therefore, once the etching broke through to the *p*-type layer, it immediately passivated. The ratio of the etching current in the *n*-type layer (10 mA) to the *p*-type layer (0.2 mA) indicated an *n*:*p* etch rate selectivity of approximately 50:1.

Next, the exposed *p*-type SiC layer and buried *n*-type material was used to determine the *p*:*n* etch rate selectivity. A second constant voltage CA etch was performed on the *p*-type layer of the same sample at an etching potential of −0.75 V ($\Delta V = -0.65$ V below the *p*-type oxidation peak). The *p*-type etch current of 2.4 mA, consistent with the current measured in the LSV, faded slowly over the measurement until it stopped after 2.5C. Although the drop in current from the *p*-to-*n* transition was less dramatic than what was observed for *n*-to-*p*, the inflection point and change in CA slope just after ∼2C of charge transfer was a clear sign of the transition into the underlying *n*-type layer. Etching into the *n*-type layer was confirmed with an LSV measurement (dark blue curve in Fig. 4a), which showed a trace nearly identical to that measured on the original *n*-type epitaxial surface. At this etching potential (−0.75 V), the difference between the etching current in the *p*-type layer (∼2 mA) and in the *n*-type layer (0.4 mA) indicated an *p*:*n* selectivity of ∼5:1. In this case, etching was performed below the oxidation peak for *n*-type. Although the current is low compared to the *p*-type current at this potential, the *n*-type layer surface did not passivate, therefore the *p*-to-*n* selectivity was much lower than what was observed for the *n*-to-*p* transition.

A cross-sectional view of the SiC pieces under scanning electron microscopy (SEM) and surface scanning profilometry confirmed the surface *n*-type layer was selectively removed during the first CA etch (at 0.47 V), exposing the underlying *p*-type layer, which was then selectively etched away upon the second CA etch (at −0.75 V), exposing the underlying *n*-type layer. Figure 5 shows SEM and profilometry characterization of the epitaxial *n*-*p*-*n* alternating layer sample before etching (as-prepared), after PEC etching of the *n*-type layer, and after etching the underlying *p*-type layer. Secondary electron yield gives regions of darker and lighter contrast associated with *n*-type and *p*-type layers, respectively. This contrast is due to a difference of the secondary electron escape depths, where the *p*-type regions emit more secondary electrons than the *n*-type regions.[26] We observed the distinct epitaxial layers including 531 nm thickness for the top *n*-type surface layer and 516 nm thickness for the *p*-type layer, followed by the *n*-type buffer. An SEM cross-section after an initial ∼3C etch at $\Delta V = -0.1$ V with respect to the *n*-type oxidation peak indicated that the surface *n*-type layer was completely removed and the thickness of the *p*-type layer was reduced by ∼70 nm, down to ∼446 nm (Fig. 5b). The cross-sections were consistent with the CA results in Fig. 4b, which showed a substantial decrease in current indicating complete removal of the *n*-type layer. The total etch time was ∼640 s, but the CA current dropped substantially after ∼400 s (indicating removal of the 531 nm thick *n*-type layer) suggesting an approximate etching rate of 78 nm min^{-1} (4.7 μm h^{-1}) for the *n*-type layer. Further characterization by surface profilometry (Fig. 5d) revealed a symmetric trench with steep walls and smooth surface at a depth of ∼600 nm with minor height non-uniformity over the 1.2 cm aperture, consistent with the SEM cross-sections (Fig. 5b). After etching, the exposed *p*-type layer was shiny optically with 0.9 nm RMS roughness from atomic force microscopy (AFM). These results confirmed the PEC etch on the top *n*-type layer caused a marginal amount of over-etching into the lower *p*-type layer and resulted in a smooth surface.

SEM indicates that the *p*-type layer was completely removed during the second etch with little-to-no damage of the underlying *n*-type layer. Figure 5c shows the SEM cross-section after the second PEC etch at −0.75 V (0.67 V below the *p*-type layer oxidation peak). At this potential the *p*-type etching occurred below the passivation peaks for both the *n*- and *p*-type SiC. The *p*-to-*n* selectivity, as determined by the ratio of the LSV currents (shown in Fig. S4), increased at lower potentials. Therefore, a lower etching potential (relative to the oxidation peak) was chosen to maximize selectivity. After etching and LSVs, the exposed *n*-type layer was also smooth and shiny and surface profilometry revealed a symmetric trench with steep walls and a flat surface at a depth of ∼1.2 μm (Fig. 5d). The total etch time for the second etch was ∼1700 s in the remaining 446 nm *p*-type layer and ∼150 nm *n*-type over-etch, suggesting an approximate etching rate of 18 nm min^{-1} (1.1 μm h^{-1}) average for the *p*-type layer. The combined time for both PEC etches was 2340 s indicating an average etch rate of ∼1.8 μm h^{-1} over the full etch depth.

The chemical reaction details were assessed by taking into account the total number of Coulombs transferred during the etching process from the CA and LSV data. The complete etch (*n*-type and *p*-type layers) required 7.98C of charge and resulted in an etch depth of 1.22 μm over an area of 1.09 cm^2. This corresponds to an etch process requiring 6.02×10^4 C cm^{-3} or 7.76 holes per formula unit of SiC. Based on Eq. 1, 6 holes are consumed during the photoelectrochemical conversion of 1 formula unit of SiC suggesting some additional charge is transferred that does not contribute to the etch process. A closer inspection of the individual layers shows that the initial *n*-type layer etch required 4.64C of charge transfer and resulted in an etch depth of 0.579 μm, which corresponds to an etch process requiring 7.14×10^4 C cm^{-3} or 9.49 holes per formula unit of SiC. The excess charge transferred during the *n*-type SiC etch may be partially associated with formation of CO_2 (rather than CO), which requires 8 holes per SiC formula unit. In addition, some water oxidation is also likely contributing to the total charge transfer during the *n*-type etch, which was performed at ∼250 mV above the thermodynamic potential for water oxidation (at pH 13). An estimation of the number of holes consumed during the *p*-type layer etch (based on the measured thicknesses for the *n*-type and *p*-type layers) is 6.0 holes per formula unit suggesting no CO_2 formation (only CO) or water oxidation occurred at this lower etch potential (−0.75 V).

Surface variation reduction with multiple etch stops.—PEC etching results suggest a high level of dopant selectivity (∼50:1 based on electrical current ratios) is possible for an *n*-to-*p* etch stop. Even higher effective selectivities (>100:1) are possible when multiple etch stops (*n*-*p*…−*n*–*p*) are coupled together and the etching potential is varied to maximize selectivity for each particular layer-to-layer transition (i.e., *n*-to-*p* and *p*-to-*n*). To better characterize the single layer selectivity and understand the limits of dopant selectivity with multiple etch stops, an *n*-*p*-*n* stack was prepared with a well-defined surface variation. Similar to previous measurements, the SiC wafer consisted of an alternating stack of epitaxial grown *n*-type and *p*-type layers on an *n*-type buffer. However, in this sample multiple 180 nm deep, 100 μm wide straight trenches were dry-etched using an inductively coupled plasma into the SiC surface with a 150 μm pitch as shown in Fig. 6a. Surface profilometry

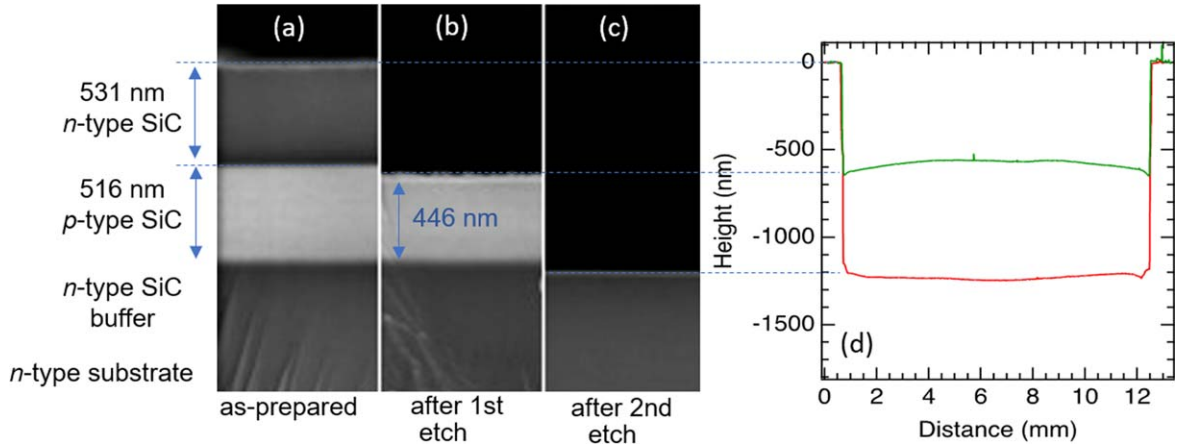

Figure 5. Characterization of selectively etched epitaxial *n-p-n* sample. SEM cross-section from a stack of alternating *n-p-n* layers (a) before and (b) after PEC etching of the *n*-type layer (∼3C) and (c) after etching the underlying *p*-type layer (∼2.5C). (d) Profilometry of the exposed surface after the first etch, resulting in the removal of the *n*-type layer (green) and after the second etch, resulting in the removal of the *p*-type layer (red). SEM images were aligned using the surface (a) and the *n-p* interface (b), with the final image aligned to the measured depth in the profilometry (c).

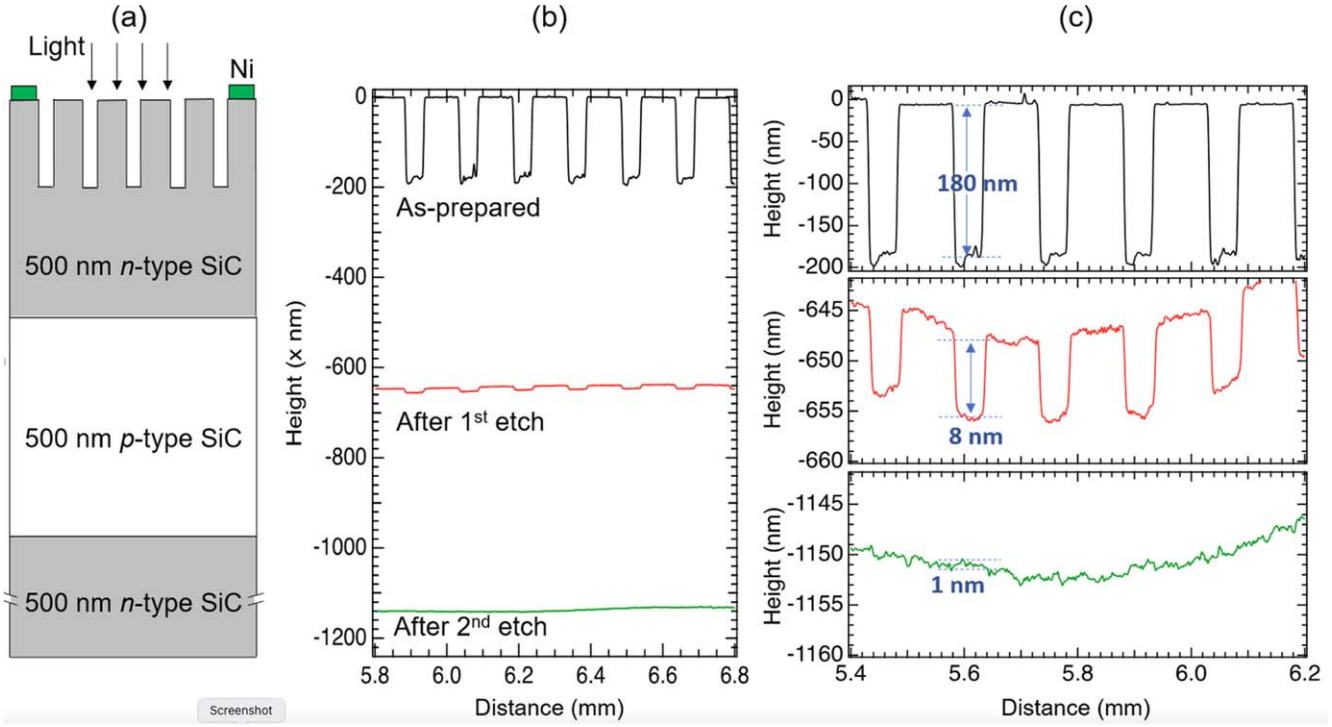

Figure 6. Dopant-selective PEC etching of an *n-p-n* epitaxial sample with periodic height variation. (a) Schematic of sample cross-section showing surface *n*-type layer prepared with 180 nm depth trenches by 100 μm wide. Drawing is not to scale. Profilometry measurements showing (b) raw data and (c) re-scaled after different stages of etching. The as-prepared surface exhibits trench heights of 180 nm (black trace), which are reduced to 8 nm after etching the top *n*-type layer (V = 0.37 V) resulting in the removal of ∼650 nm SiC on average (red trace). After etching the *p*-type layer (V = −0.75 V) resulting in the removal of another ∼500 nm, the trenches were no longer clearly visible (green trace) with nanometer scale height variation.

measurements before PEC etching are shown in the black trace in Fig. 6b (at scale) and Fig. 6c (expanded). The trench depths pre-etch and post-etch were used to directly measure the physical etch rate selectivity.

The trenched sample was selectively PEC etched using LSV and CA analogous to the sample described in Fig. 4. Initial LSV measurements on the *n*-type surface layer (Fig. S5a) showed an oxidation peak at ∼0.47 V similar to previous measurements (Fig. 4a). A first PEC etch on the trenched *n*-type surface was performed at 0.37 V, 0.1 V below the *n*-type peak. The CA (Fig. S5b) shows an initial current of ∼7.5 mA, which dropped slowly to 6 mA over ∼2.5C of charge transfer (∼500 s). A reduction in current was expected as the etching at the bottom of the trenches transitioned into the *p*-type layer. After ∼ 2.6C of total charge transfer the current dropped off and leveled off to 0.2 mA indicating a complete transition into the *p*-type layer. At 0.37 V the current measured on the *n*-type surface was ∼37x larger than that measured on the *p*-type layer. Surface profilometry shown in the red trace in Figs. 6b, 6c reveals a reduction in step height from 180 nm down to 8 nm, yielding a selectivity of ∼22:1. The curvature (long-range surface variation) evident in the middle and lower panels of Fig. 6c is associated with wafer bow, which is present in the as-prepared wafer (as shown in Fig. S6) and is not attributed to additional surface variation introduced by PEC.

The *n*-to-*p* etch was subsequently followed up with a *p*-to-*n* etch so that the net surface variation reduction was multiplicative in their etch rate selectivities. LSV on the exposed *p*-type surface layer (Fig. S5a) showed an oxidation peak at about −0.1 V, which was similar to previous measurements (Fig. 4a). PEC etching on the *p*-type surface with ∼8 nm trenches was performed at −0.75 V (0.65 V below the *p*-type oxidation peak). The CA reveals an initial current of ∼2 mA, which dropped slowly to 0.4 mA over ∼3.1C of charge transfer in ∼2600 s. Similar to the first etch, a reduction in current was expected as the etching at the bottom of the trenches transitioned into the *n*-type layer. At −0.75 V the current measured on the *p*-type surface was ∼5x larger than that measured on the *n*-type surface. Surface profilometry reveals a reduction in step height from 8 nm down to 1 nm, for a selectivity of ∼8:1. The surface roughness measured by AFM over a 5 × 5 μm^2 scan after the final etch gave an RMS roughness of 1.2 nm (1.0 nm) in a region inside (outside) the PEC etched area (Table SI). These results are consistent with the profilometry (green trace in Fig. 6c) and confirm that the PEC etching produces a surface with low roughness (∼1 nm). More broadly, this investigation demonstrates that dopant-selective PEC etching is capable of reducing the total thickness variation of SiC by 180:1 (180 nm → ∼1 nm) with only two etch stops. Surface planarization and local roughness could further be improved with a short chemical-mechanical polish.

Summary

The next generation of SiC nanophotonic structures will require new methods to etch and isolate SiC with low-defect-densities and low TTV (⩽10 nm) to limit propagation loss and to maintain high coupling efficiency to other elements. Additionally, commercial epitaxial grown SiC layers may host optically addressable defect spins for quantum technologies. Given the typical TTV >1 μm present after grinding and polishing, a significant reduction in TTV is necessary to produce smooth planar surfaces necessary for photonic devices without introducing unrecoverable subsurface damage. We proposed a new method to prepare defect-free single crystalline 4H-SiC on insulator with nanometer-scale precision based on photoelectrochemical etching. This method requires a wet etching process that is fast (⩾1 $\mu m\ h^{-1}$), wafer-scalable, and has an effective selectivity of ⩾100:1. Our process achieves these requirements and produces a smooth, non-porous surface (nanometer-scale roughness) with uniform etching across the etched area.

We demonstrated an effective selectivity of 180:1 using 2 sacrificial etch stop layers on an artificially stepped surface. In addition, surface profilometry revealed very low surface roughness (⩽1 nm RMS) and no obvious porosity formed under optimal etching conditions. This effective selectivity could be increased by etching the *p*-type layer at a lower potential. For example, linear sweep voltammetry suggests a *p*-type layer selectivity (based on a current ratio) of 20:1 (for an overall effective selectivity of ∼400:1) is possible with a 50% reduction in the etching current for the *p*-type layer. Similarly, the effective selectivity could also be increased by incorporating additional sacrificial layers. For example, a wafer with at least 3 sacrificial layers (e.g. *n*-*p*-*n*-*p*) would exhibit an effective selectivity >4000:1, suggesting a possible TTV reduction from 10 μm down to sub-10 nm where new limitations of TTV would be reached such as the epitaxial growth uniformity on thin layers.

In addition to high selectivity and low roughness, we demonstrated this process is practicable and scalable to larger wafers. Rates as fast as 4.7 $\mu m\ h^{-1}$ for the *n*-type layer and 1 $\mu m\ h^{-1}$ for the *p*-type layer were characterized over 2 sacrificial layers. Faster PEC etch rates may be possible while maintaining good etch rate selectivity by exploring different electrolyte concentrations, higher light intensities, or varying setup conditions. The *p*-type layer rates could be further increased by etching at higher potentials, closer to the peak, but this would also result in reduced selectivity for that layer. Although the PEC etching in this study was performed over a relatively small area (1.3 cm^2), all methods are straightforward to accommodate larger wafer diameters (e.g. 2 or 4 inches). In order to maintain smooth and uniform etching, it is critical the light is capable of illuminating the surface with sufficient intensity to generate a passivation peak (e.g. Figs. 3, 4) to ensure high selectivity. In addition, the light intensity must be constant across the full wafer to ensure uniform etching. Finally, the electrolyte must be circulated to ensure a constant and uniform temperature across the wafer.

For wafer-scale low TTV SiCOI fabrication the SiC wafer needs to be flipped and wafer bonded to an oxide layer, which exposes the opposite face as the process side. The substrate is then mechanically grinded and polished to remove a majority of material before the doped sacrificial layers must be PEC etched away. Most commercially available SiC wafers are epitaxial grown on the Si-face, which necessitates PEC etching of the C-face. The work presented here was performed on the Si face (0001) of SiC. Further work is necessary to establish a similar process for the SiC C-face ($000\bar{1}$). Alternatively, a C-face epitaxial grown SiC wafer can be bonded and ground down from the Si-face side, to use this work's demonstrated selectivity.

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ORCID

Jason Graetz https://orcid.org/0000-0002-2584-2357

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